High-Efficiency GaAs-Based pHEMT C-Band Power Amplifier

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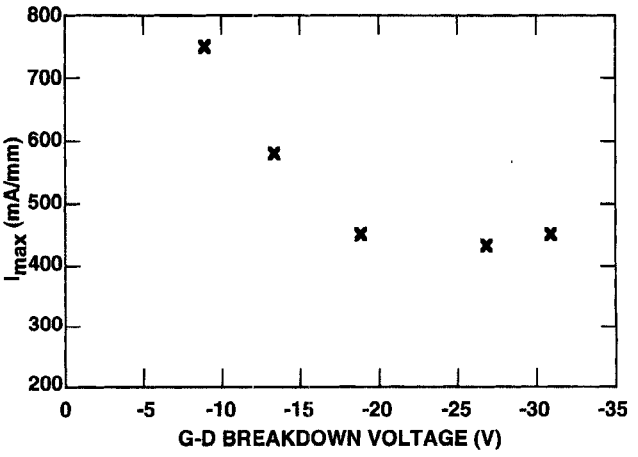
Abstract— **A high-efficiency C-Band power amplifier design utilizing AlGaAs/InGaAs/GaAs pHEMT's is reported. On-wafer active loadpull power measurements at 4.5 GHz of a $0.25\mu m \times 1.2$ mm pHEMT exhibited an output power of 0.35 W and power-added efficiency of 79%. A single-stage MIC amplifier fabricated with a 2.8-mm-wide pHEMT resulted in P_{out} = 1.2 W and PAE = 74% at 4 GHz. These results demonstrate the potential of pHEMT's to significantly improve the efficiency performance of microwave solid state power amplifiers compared to present MESFET designs.**

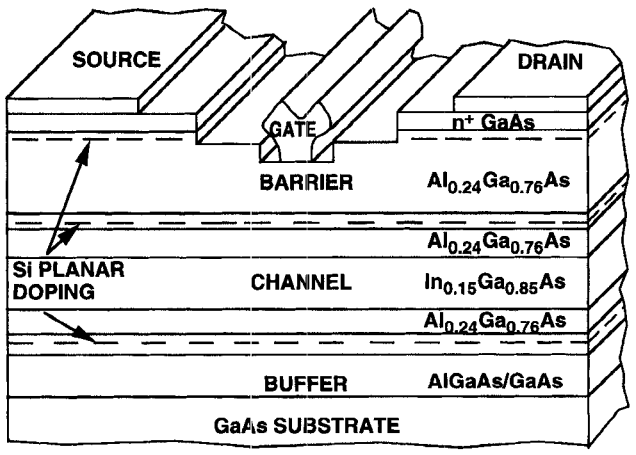
I. Introduction

HIGH-EFFICIENCY power transistors are a critical building block of solid-state power amplifiers (SSPA's) for applications such as satellite communications systems. Even though there is new emphasis for satellite applications involving television broadcast at higher operating frequencies (i.e., Ku- and K-band), there is still a great need for improved performance of transponders at lower frequencies (i.e., C-Band) (1). There exist additional high-performance, high-volume space applications at even lower frequencies (L- and S-Band) for new wide-area mobile communications systems. The GaAs-based metal-semiconductor field effect transistor has been considered the baseline power device for current C-Band SSPA applications [2], [3]. The potential for higher efficiency performance of heterojunction-based (HJ) devices, such as the pseudomorphic high electron mobility transistor pHEMT and the heterojunction FET (HFET), has resulted in significant interest in the HJ device technology for both microwave and millimeter-wave power applications (i.e., [4]–[6]).

To achieve high power and efficiency simultaneously, a high breakdown voltage is required. The initial limitation of the HJ FET's at microwave frequencies was a characteristic low gate-drain breakdown voltage (i.e. $BV_{gd} < -10$ V). Researchers have implemented a double gate recess process [7] to increase the breakdown voltage competitive with the MESFET technology. A figure of merit for power FET's commonly used is the product of gate-drain breakdown voltage (BV_{gd}) and full channel current (I_{full}). A comparison of data achieved in our laboratory for different epitaxial layer designs to vary the maximum channel current, and therefore BV_{gd}, is shown in Fig. 1(a). These passivated pHEMT's were all processed in our laboratory with the same fabrication steps and the only variables were the sheet charge and both composition and thickness of the $In_xGa_{1-x}As$ channel layer. By reducing the doping and In composition from 3.4×10^{12} cm^{-2} and 22% to 2.4×10^{12} cm^{-2} and 15%, respectively, a reproducible breakdown voltage of $|BV_{gd}| > 20$ V is obtained. In this letter, the amplifier results obtained using this high breakdown voltage pHEMT device technology are reported.



(a)



(b)

Fig. 1. (a) Cross section of pHEMT device structure and (b) variation of the device gate-drain breakdown voltage with maximum channel current.

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II. Device Structure and Fabrication

The pHEMT structure reported in this work and shown in Fig. 1(b) was grown by molecular beam epitaxy (MBE). The structure is a triple-doped $Al_{0.24}Ga_{0.76}As/In_{0.15}Ga_{0.85}As/GaAs$ pHEMT with two of the doping layers to supply the charge to the channel and the third Si-doping plane under the n^+ GaAs contact cap layer to minimize access resistance. The double modulation doping scheme was implemented to achieve a sheet charge of $n_s \sim 2.5 \times 10^{12}\,cm^{-2}$. The measured room temperature Hall sheet charge and mobility for this structure are $2.38 \times 10^{12}\,cm^{-2}$ and $6700\ cm^2/V-s$, respectively.

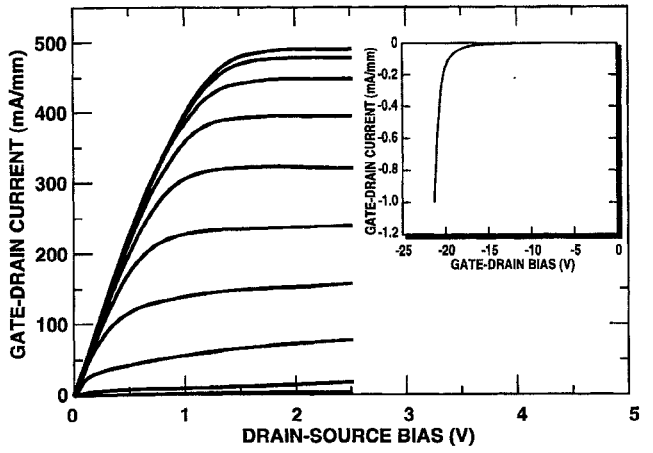
The device fabrication process begins with deposition of Ni/AuGe/Ag/Au source-drain ohmic contacts. A boron implantation process is then used to isolate the active region. Next, the ohmic contacts are alloyed at 420 C for 30 seconds in a forming gas ambient. A specific contact resistance of 0.25 ohm-mm was obtained for this structure as compared to 0.32 ohm-mm for the double doped layer design. The gate recess process was then performed by a two-step nonselective etch process using a citric-acid based etchant. A source-drain spacing of 3 μm and channel recess width of 1.5 μm were found to result in the best combined dc and rf performance. The double recess etch process was developed using atomic force microscopy (AFM) to identify a reproducible wet chemistry and calibrate the resultant etch rate (8). The 0.25-μm gates were formed by e-beam lithography and deposition of Ti/Pt/Au metalization. Finally, a 1000-Å layer of silicon nitride was deposited for device passivation and air-bridge interconnect metal fabricated. The wafer was thinned to 35 μm to reduce the thermal resistance and backside vias formed to minimize source inductance.

III. Device and Amplifier Performance

Devices were fabricated with total gate periphery of 0.4–19.8 mm. Fig. 2(a) shows the I-V characteristics of a $0.25\,\mu m \times 0.4\,\mu m$-wide pHEMT. The dc performance is characterized by a maximum transconductance of 280 mS/mm, $I_{full} = 490$ mA/mm, and gate-drain breakdown voltage (source floating) of $|BV_{gd}| = 21.5$ V measured at $|I_{gd}| = 1$ mA/mm [see inset to Fig. 2(a)].

On-wafer power measurements were performed using an active load-pull CW measurement system [9] at 4.5 GHz. The measurement system is designed with independently adjustable loads to terminate the fundamental, second, and third harmonics for this measurement frequency. Devices with gate periphery of 1.2 mm were characterized with this system. The data was taken before the wafer was thinned or backside vias fabricated. Since the measurement was CW, sufficient power dissipation of the devices was of concern. However, the lateral and vertical path through the wafer for heat dissipation provided adequate heat sinking for the power levels reported here. The devices were biased at ~10% of I_{full} for Class A-B operation. Drain-source bias was studied to optimize power-added efficiency (PAE) and output power (P_{out}).

A plot of the on-wafer measured output power and PAE as a function of input power for $V_{ds} = 5$ V is shown in Fig. 2(b). A



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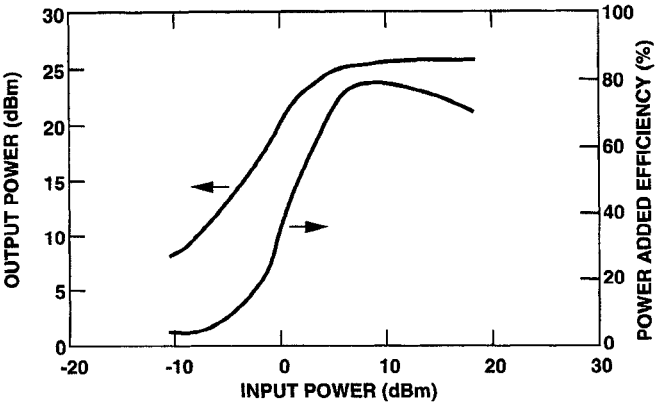
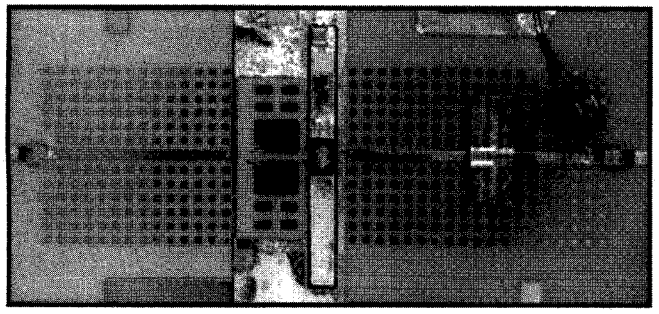


(b)

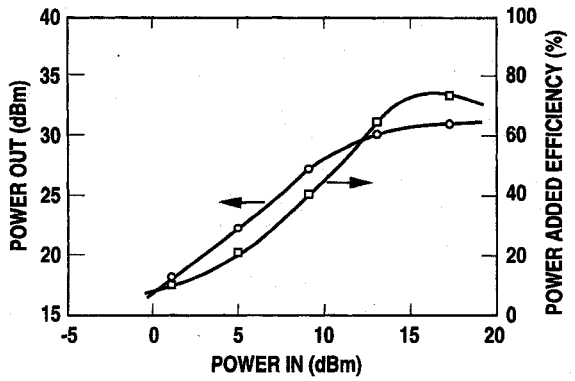
Fig. 2. (a) IV characteristic for a $0.25 \times 400\,\mu m^2$ pHEMT device and the gate-drain breakdown voltage curve. Here V_{gs} is varied from +1.0 V to −1.25 V in steps of −0.25 V. (b) On-wafer active load pull measurement if a $0.25 \times 1200\,\mu m^2$ pHEMT device demonstrating maximum efficiency and output power of 79% and 0.35 W, respectively.

maximum PAE of 79% is obtained at $P_{out} = 25.4$ dBm (0.35 W, 0.29 W/mm). An improvement in of 8–10% was obtained by tuning the second harmonic (9 GHz) and 2–3% for the third harmonic (13.5 GHz) tuning. The data obtained with this measurement system assumes a conjugate input match for the device. Increasing V_{ds} to 7 V resulted in a significant increase of output power with a small decrease in PAE. Here, for $V_{ds} =$ 7 V, the measured data were PAE = 76%, $P_{out} = 28.1$ dBm (0.65 W, 0.54 W/mm).

The load impedances measured for the 1.2-mm-wide pHEMT were scaled to estimate the optimum load impedances for a single-stage power amplifier with the 2.8-mm-wide device. The device technology demonstrated good power density scaling. In addition, the 2-terminal gate-drain breakdown voltage of the wider parts was comparable to the smaller gate periphery devices. A photograph of the 2.8-mm pHEMT amplifier is shown in Fig. 3(a). The measured RF power performance of this amplifier operating at 4 GHz is shown in Fig. 3(b). The measured output power at $V_{ds} =$ 8 V was 30.8 dBm (1.2W, 0.43 W/mm) with PAE = 74%.



(a)



(b)

Fig. 3. (a) Photograph of a 2.8-mm gate periphery pHEMT amplifier and (b) the measured efficiency and output power for this amplifier.

The output power for the 1.2 and 2.8 mm pHEMT amplifiers does not scale with device size since the biasing and tuning of the parts was not the same. The fundamental load impedance presented to the amplifier for best performance, however, scales well from the on-wafer result. In this initial circuit, the second and third harmonic terminations were close to the on-wafer values but not exactly the same. All efforts were made to minimize circuit losses in the rf and dc circuitry. Damping circuitry was used to make the amplifier critically stable in-band ($K = 1, B_1 > 0$). A two-tone linearity measurement was made on the amplifier. For a two-tone input power equal to that needed to obtain maximum single carrier efficiency as above and with 2-MHz carrier spacing, the carrier to intermod (C/3IM) ratio was 14 dBc. All of the quoted amplifier numbers were made in a system calibrated from coaxial connector to connector with the V_{ds} measurement made at the bias probe external from the circuit.

IV. Conclusion

A high breakdown voltage GaAs-based pHEMT device technology has been reported. To the best of our knowledge, the reported on-wafer PAE of 79% for $P_{\text{out}} = 0.35$ W is the highest-reported efficiency for a GaAs-based pHEMT operated at 4.5 GHz. The fabricated power amplifier obtained $P_{\text{out}} = 1.2$ W with PAE of 74% at 4 GHz. This amplifier result, while slightly lower in efficiency than the on-wafer result (primarily due to matching circuit losses), represents a higher power density. Currently, amplifiers with single devices of total gate peripheries up to 25 mm are being fabricated. An output power of $\approx$15 W and efficiencies approaching 70% are predicted based on the performance reported in this letter.

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